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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/473,305 12/28/99 FRUTSCHY

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EXAMINER

MMC1/1012

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PARENTH. N
ART UNIT

PAPER NUMBER

2811
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/473,305

Applicant(s)

Frutschy et al

Examiner

Nitin Parekh

Group Art Unit
2811



☒ Responsive to communication(s) filed on Aug 16, 2000

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-28 is/are pending in the applicat

Of the above, claim(s) 8-11 and 17-22 is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-7, 12-16, and 23-28 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

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DETAILED ACTION

Claim Objections

1. Claims 25-27 are objected to because of the following informalities:

The claim numbers have been repeated in claim 25. Claims 25-27 should be renumbered as claims 25-28 in the ascending order.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-7, 12-16 and 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree (US Pat. 5783461) in view of Domadia et al (US Pat. 5949137).

Regarding claim 1, Hembree discloses a microelectronic component assembly comprising:

- a first substrate having a first and second surface and the first surface including contacts

(microelectronic device substrate 12, Fig. 2)

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- a second substrate having a first and second surface and the first surface including contacts (interposer substrate 16, Fig. 2)
- microbumps/solder balls extending between the first and second substrate contacts where the microbumps/solder balls are attached to the second substrate contact (bumps 60B-Fig. 5A; Fig. 4-6; Col. 6, line 21- 65), and
- a compression mechanism/support structure for imparting pressure between the first and second substrate (18 and 26 in Fig. 1 and 2; Col. 3, line 35) (Fig. 1-10; Col. 1, line 55- Col. 6, line 65).

Hembree fails to specify using microbumps/solder balls attached to the first substrate contact. However, it is conventional in the chip interconnection technology art to attach the solder balls/bumps on any substrate such as die, carrier, interposer, etc. to meet the interconnection, testing and design requirements. The cited reference by Farnworth et al teach using solder ball placement interchangeably on die or carrier substrate (Col. 4, line 10) to meet the interconnection requirements. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate solder balls attached to the second substrate contact to meet electrical testing and design requirements in Hembree's assembly as cited in claim 1.

Regarding claims 2-4, Hembree discloses the first substrate comprising a microelectronic package/carrier substrate/microelectronic device (Fig. 2; Col. 1, line 55- Col. 4, line 47).

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Regarding claim 5, Hembree discloses a second substrate contact/non-reflow electrical contact comprising a recess defined by sidewalls (vertical and inclined) extending into second substrate and conductive material layered in the recess (Fig. 5 and 5A; Col. 6, line 34-65).

Regarding claims 6 and 7, Hembree fails to specify the dimensions such as a width and shape of second substrate contact being same as a diameter of the solder ball and shape of a semispherical surface of same radius as that of the solder ball respectively. The parameters such as length, width, depth, shape/angle of the recessed area, volume of the void in the recess, etc. of the contact pad/area in the chip interconnection technology art are considered to be a matter of design choice. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate width and shape of second substrate contact being same as a diameter of the solder ball and shape of a semispherical surface of same radius as that of the solder ball to meet the design requirements in Hembree's assembly as cited in claims 6 and 7 respectively.

Claim 12 is rejected as explained above for claim 1.

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Regarding claims 13 and 14, Hembree discloses compression mechanism/support structure comprising:

- a frame portion (portion 36 in Fig. 2) of the base
- a backing plate/strip (strip 31 in Fig. 2) abutting the second surface second surface
- a cover plate/thermal plate (plate 24 in Fig. 2) extending over the frame portion and adjacent to the first substrate
- a resilient elastomeric spacer ring/washer spring (washer 22 in Fig. 2) extending between the thermal plate and the microelectronic device/interposer substrate, and
- plurality of retention devices such as clips and clamps

(Fig. 1-10; Col. 1, line 55- Col. 6, line 65).

Hembree fails to specify the retention devices comprising a plurality of bolts and nuts extending through the backing plate, frame and thermal plate. Domadia et al teach using a support structure where the plurality of retention devices having a plurality of bolts and nuts extending through the back of the substrate, stiffener/frame portion and thermal plate/heat dissipater (Fig. 5-7; Col. 4, line 40-Col. 6, line 48). Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the retention devices comprising a plurality of bolts and nuts extend extending through the backing plate, frame and thermal plate to reduce the mechanical stress on the device using Domadia et al's retention device Hembree's assembly as cited in claims 13 and 14.

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Regarding claim 15, Hembree discloses the first substrate comprising a microelectronic device package including a microelectronic device attached to and in electrical contact with a first surface of an interposer/multilayered TAB tape with multilayer contact surfaces where the first substrate first contact comprises contacts on a second surface of the interposer substrate (Fig. 2-5A; Col. 6, line 21- Col. 6, line 65; Col. 1, line 55- Col. 4, line 47).

Claim 16 is rejected as explained above for claims 12-14.

Claims 23 and 24 are rejected as explained above for claims 5 and 1.

Claims 25 and 26 are rejected as explained above for claims 24, 23, 6, 5, 1 and 23, 7, 5, 1 respectively.

Regarding claim 27, as explained above for claims 23-26, Hembree discloses a second substrate contact/non-reflow electrical contact comprising a recess defined by sidewalls (vertical and inclined) extending into second substrate and conductive material layered in the recess (Fig. 5 and 5A; Col. 6, line 34-65). Hembree fails to specify using a resilient material disposed between the substrate and the conductive material layer. It is conventional in the chip interconnection technology art to use additional resilient material layers under conductive material layer to improve the interconnection reliability. The cited reference by Abram teaches using such layers

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(Fig. 3c and 3d; Col. 5 and 6) for the substrate contact. Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate a resilient material disposed between the substrate and the conductive material layer to meet design and reliability requirements in Hembree's assembly as cited in claim 27.

Claim 28 is rejected as explained above for claims 1, 5-7 and 23-27.

Papers related to this application may be submitted directly to Art Unit 2811 by Facsimile transmission. Papers should be faxed to Art Unit via Tech Center 2800 fax center located in Crystal Plaza 4, Room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh at (703) 305-3410. The examiner can normally be reached on Monday-Friday from 08:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

10-06-00

Steven Loke
Primary Examiner

